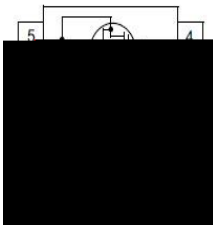
Product Summary

The ZMD68310M combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. Two N Channel MOSFET inside for dual DIE implication.

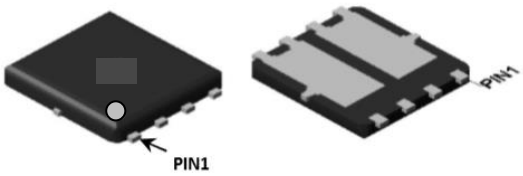


A density Trench technology

$_{DS(ON)}$ to minimize conductive loss

G , C , ,

Dual DIE in one package



Power Management in Notebook Computer

BLDC Motor driver

Absolute Maximum Ratings T_C =25

Parameter	**Symbol**	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current	$I_{D@}$TC=25		
	$I_{D@}$TC=75		
	$I_{D@}$TC=100		
Pulsed Drain Current	I_{DM}	36	A
Total Power Dissipation(TC=25)	P_D@TC=25	3.2	W
Total Power Dissipation(TA=25)	P_D@TA=25	0.65	W
Operating Junction Temperature	T_J	-55 to 150	
Storage Temperature	T_{STG}	-55 to 150	
Single Pulse Avalanche Energy	E_{AS}	65	mJ

Test Circuit

Fig.1 Switching Time Measurement Circuit

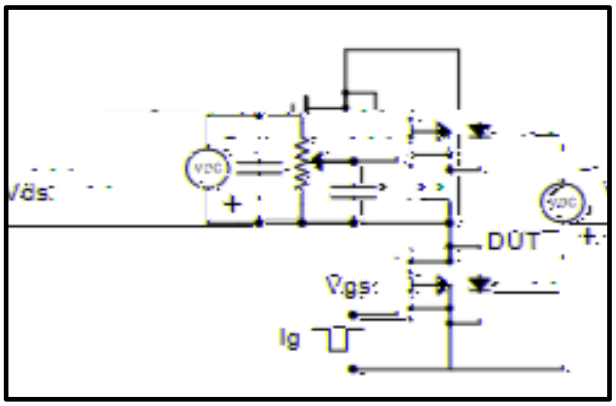


Fig.2 Gate Charge Waveform

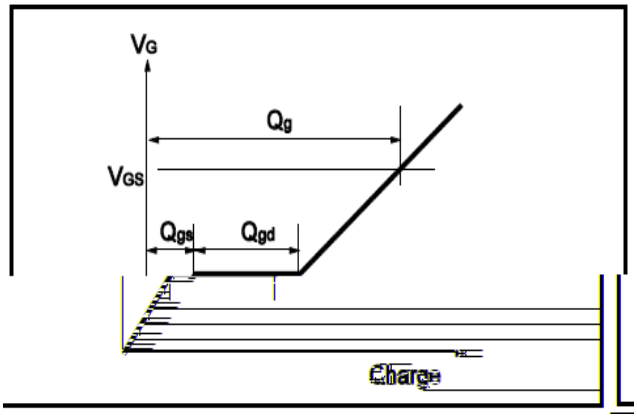


Fig.3 Switching Time Measurement Circuit

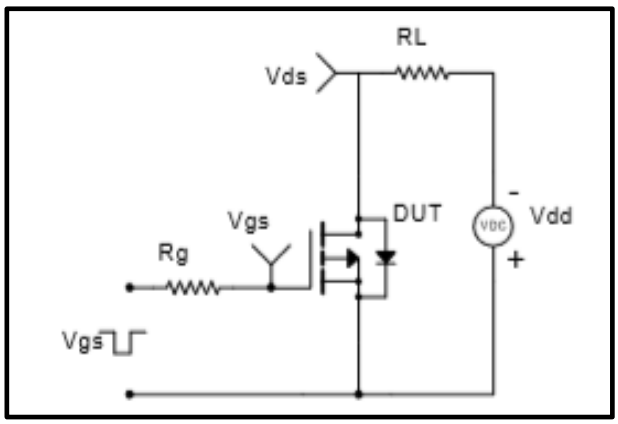


Fig.4 Gate Charge Waveform

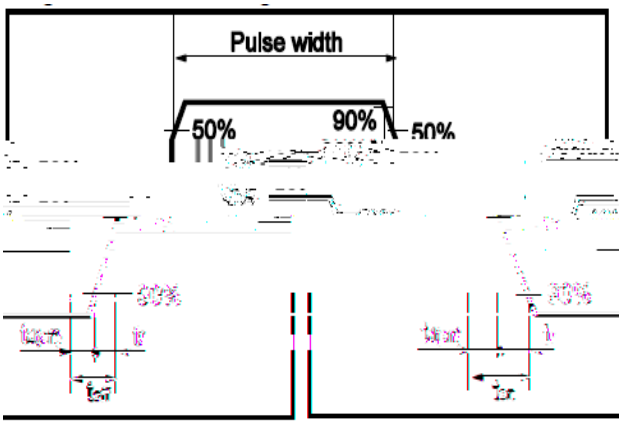


Fig.5 Avalanche Measurement Circuit

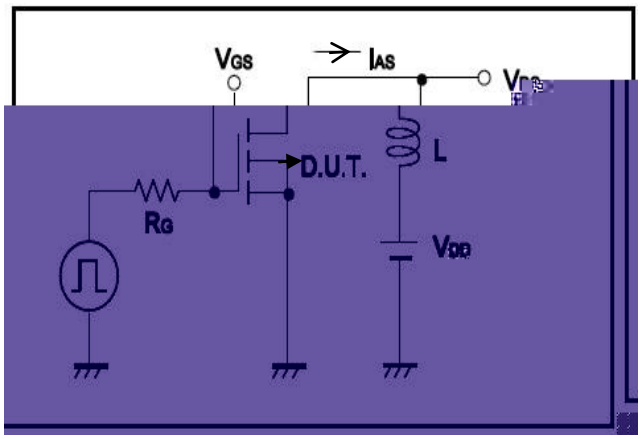
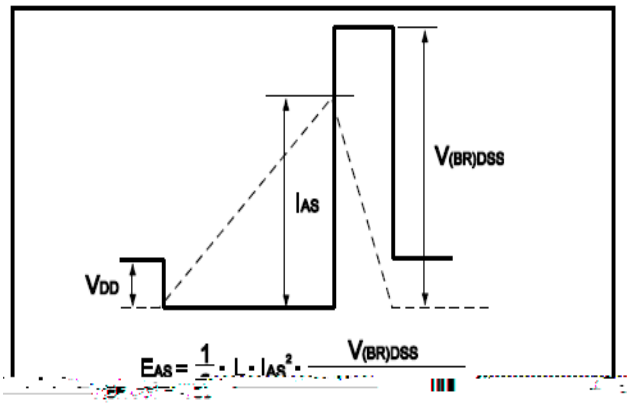
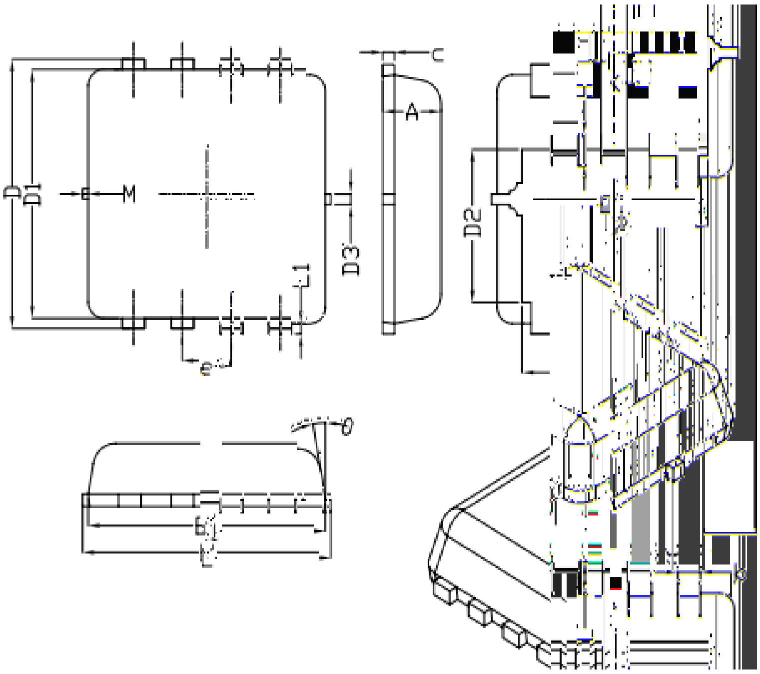


Fig.6 Avalanche Waveform



sions DFN5×6

Unit mm



SYMBOL	DIMENSIONAL REQMTS MIN	NOM	MAX
A	0.70	0.75	0.80
b	0.25	0.30	0.35
c	0.10	0.15	0.25
D	[illegible]	[illegible]	[illegible]
D1	[illegible]	[illegible]	[illegible]
D2	[illegible]	[illegible]	[illegible]
D3	---	0.13	---
E	3.20	3.30	3.40
E1	3.00	3.15	[illegible]
E2	[illegible]	[illegible]	[illegible]
e	0.65BSC		
H	0.30	0.39	0.50
L	0.30	0.40	0.50
L1	---	0.13	---
K	[illegible]	[illegible]	[illegible]
θ	[illegible]	[illegible]	[illegible]
M	[illegible]	[illegible]	[illegible]

* Not specified